METHOD FOR MANUFACTURING METAL LINE OF SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to method for manufacturing metal line of semiconductor device, and in particular to an improved method for manufacturing metal line of semiconductor device wherein undesirable etching of an edge of an interlayer insulating film which causes electrical shorts between metal lines can be prevented.

2. Description of the Background Art

A semiconductor device includes a plurality of vertically stacked electrical wiring layers and connection layers connecting vertically stacked electrical wiring layers.

In case of logic devices, gates and metal layers correspond to the electrical wiring layers, and contact hole layers connecting gates and metal layers and via contact hole layers connecting an upper and a lower wiring layers correspond to the connection layers.

In accordance with a conventional method for manufacturing metal line of semiconductor device, a metal

line is formed on a planarized surface and an interlayer insulating film planarizing the entire surface is then formed. However, this method is disadvantageous in that the patterning of metal lines having microscopic widths is very difficult.

A new method, namely a damascene method wherein a interlayer insulating film having a groove for metal line is formed on a planarized surface and the groove is filled with metal have been proposed to overcome the disadvantages of the conventional method, which is described hereinbelow.

Figs. 1a through 1e are cross-sectional diagrams illustrating a conventional damascene method for manufacturing metal line of semiconductor device.

Referring to Fig. 1a, a lower structure such as a device isolation film (not shown) defining an active region, a word line (not shown), a bit line (not shown) and a capacitor (not shown) are formed on a semiconductor substrate (not shown). A lower insulating layer (not shown) is deposited to planarize the entire surface.

Thereafter, a lower metal line 11 connected to the lower structure is deposited on the lower insulating layer using copper. A first insulating film 13 exposing a top surface of the lower metal line 11 is then formed on the entire surface.

Next, a stacked structure of a first etch barrier film

15, a second interlayer insulating film 17, a second etch barrier film 19, a third interlayer insulating film 21 and a hard mask layer 23 is formed on the entire surface. The stacked structure is then etched via a photolithography process using metal line contact mask (not shown), i.e. via contact mask (not shown) to expose the first insulating film 13.

Now referring to Fig. 1b, an organic anti-reflection film 27 is deposited on the entire surface. Thereafter, a photoresist pattern 29 is formed on the organic anti-reflection film 27. The photoresist pattern 29 is formed via exposure and development process using metal line mask.

Referring to Fig. 1b, the organic anti-reflection film 27, the hard mask layer 23 and the third interlayer insulating film 21 are etched using the photoresist pattern 29 as a mask to expose the second etch barrier film 19. The organic anti-reflection film 27 remains between the second interlayer insulating film and the first etch barrier film 15.

Now referring to Fig. 1d, the photoresist pattern 29 and the organic anti-reflection film 27 are sequentially removed to expose the first etch barrier film 15 on the lower metal line 11.

Referring to Fig. 1e, the exposed portion of the first etch barrier film 15 is removed via an etch-back process to

form an upper metal line region 31 for contacting the lower metal line 11. The etch-back process is performed without using a mask, wherein the edges of the second etch barrier film 19, the second interlayer insulating film 17, and the hard mask layer 23 are etched to have a shape denoted as 'A' in Fig. 1e.

The edges having the shape denoted as 'A' in Fig. 1e has an effect of reducing the distance between the upper metal lines to cause shorts between the upper metal lines. The short between the upper metal lines degrades the electrical characteristic of metal lines.

Fig. 2 is a SEM photograph showing copper lines manufactured in accordance with the conventional method. As can be seen from Fig. 2, the critical dimension between the copper lines is reduced.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method for manufacturing metal line of semiconductor device wherein a lower metal line exposed through a via contact hole is covered by a photoresist pattern so that the edge of an interlayer insulating film at the top corner of the via contact hole is not etched during a formation process of upper metal line region to prevent

the reduction of distance between metal lines which causes short between the metal lines.

In order to achieve the above-described object of the invention, there is provided a method for manufacturing metal lines of semiconductor device, the method comprising the steps of: forming a first interlayer insulating film exposing a top portion of a lower metal line on a semiconductor substrate; forming a stacked structure of a first etch barrier film, a second interlayer insulating film, a second etch barrier film, a third interlayer insulating film and an anti-reflection film; etching the stacked structure to form a via contact hole exposing a portion of the first interlayer insulating film on the lower metal line; removing the exposed portion of the first interlayer insulating film to expose the lower metal line; forming a photoresist film on the entire surface; subjecting the photoresist film to an exposure and development process using an upper metal line mask to form a photoresist film pattern for defining an upper metal line region, wherein the photoresist film pattern further fills a portion of the via contact hole; etching the anti-reflection film and the third interlayer insulating film using the photoresist film pattern as a mask to form the upper metal line region; removing the photoresist film pattern; and forming an upper metal line contacting the lower metal line by filling the

upper metal line region.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become better understood with reference to the accompanying drawings that are given only by way of illustration and thus are not limitative of the present invention, wherein:

Figs. 1a through 1e are cross-sectional diagrams illustrating a conventional damascene method for manufacturing metal lines of semiconductor device.

Fig. 2 is a SEM photograph showing metal lines manufactured in accordance with the conventional method.

Figs. 3a through 3e are cross-sectional diagrams illustrating a method for manufacturing metal lines of semiconductor device in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A method for manufacturing metal line of semiconductor device in accordance with a preferred embodiment of the present invention will now be described in detail with reference to the accompanying drawings.

Figs. 3a through 3e are cross-sectional diagrams

illustrating a method for manufacturing metal lines of semiconductor device in accordance with the present invention.

Referring to Fig. 3a, a lower structure such as a device isolation film (not shown) defining an active region, a word line (not shown), a bit line (not shown) and a capacitor (not shown) are formed on a semiconductor substrate (not shown). A lower insulating layer (not shown) is then deposited to planarize the entire surface.

Thereafter, a lower metal line 41 connected to the lower structure is deposited on the lower insulating layer preferably using copper. A first insulating film 43 exposing a top surface of the lower metal line 41 is then formed to planarize the entire surface.

Next, a first etch barrier film 45 is formed on the entire surface. The first etch barrier film 45 serves as a capping layer for copper and preferably comprises an insulating film, for example SiN film, SiC film or SiCN film.

Still referring to Fig. 3a, a second interlayer insulating film 47 is formed on the first etch barrier film 45. In one embodiment, the second interlayer insulating film 47 preferably comprises a film selected from the group consisting of an oxide film, an organic low-k film, an organic porous low-k film and combinations thereof. In another embodiment, the second interlayer insulating film 47

preferably comprises a silica-base low-k film or a silica-base porous low-k film.

Thereafter, a second etch barrier film 49 and a third interlayer insulating film 51 are sequentially deposited on the second interlayer insulating film 47. The third interlayer insulating film 51 preferably consists of the same material as the first etch barrier film 45.

Next, an anti-reflection film 53 is formed on the third interlayer insulating film 51. Preferably, the anti-reflection film 53 comprises SiON inorganic anti-reflection film. The thickness of the anti-reflection film 53 is determined by considering the thickness of the anti-reflection film 53 etched during the etching process of the first and the second etch barrier films. For example, when an anti-reflection film 53 having a thickness of 600Å is required and thickness of about 400Å is etched during the etching process, initial thickness of the anti-reflection film 53 should be about 1000Å.

The anti-reflection film 53, the third interlayer insulating film 51, the second etch barrier film 49 and the second interlayer insulating film 47 are etched via a photolithography process using metal line contact mask (not shown), i.e. via contact mask (not shown) to form a via contact hole 55 exposing the first insulating film 45.

Referring to Fig. 3b, the exposed portion of the first

insulating film 45 at the bottom of the via contact hole 55 is removed via an etching process. Portions of the anti-reflection film 53, i.e. a top and edge portions of the anti-reflection film 53 are etched in the etching process of the first insulating film 45. As a result, the thickness of the anti-reflection film 53 is reduced and the edge portion of the anti-reflection film 53 at the top corner of the via contact hole 55 is etched to have a shape denoted as 'B' in Fig. 3b.

Now referring to Fig. 3c, a photoresist film (not shown) is formed on the entire surface and the photoresist film is exposed and developed using a metal line mask (not shown) to form a photoresist film pattern 59. A portion of the photoresist film remains at the bottom of the via contact hole 55 so that the photoresist film pattern 59 covers the lower metal line 41.

When the photoresist film pattern 59 at the bottom of the via contact hole 55 does not sufficiently fill the bottom of the via contact hole 55, i.e. when the thickness of the photoresist film pattern 59 at the bottom of the via contact hole 55 is not sufficient, the lower metal line 41 may be damaged or contaminated in the subsequent etching process. In order to prevent the damage or contamination of the lower metal line, the photoresist film pattern 59 at the bottom of the via contact hole 55 should have a sufficient

thickness.

Referring to Fig. 3d, the anti-reflection film 53 and the third interlayer insulating film 51 are etched using the photoresist film pattern 59 as a mask to form upper metal line region 61. It is preferable that the anti-reflection film 53 and the third interlayer insulating film 51 are plasma-etched using a mixture gas of $CF_4/O_2/Ar$.

Referring to Fig. 3e, the portion of the photoresist film pattern 59 in the via contact hole 55 is removed preferably by performing an in-situ plasma-etching process using a mixture gas of $CF_4/O_2/Ar$. The remaining portion of the photoresist film pattern 59 is then removed. Edge portions of the anti-reflection film 52 and the second etch barrier film 49 in the upper metal line region 61, which are denoted as 'C' in Fig. 3e, are not etched.

Thereafter, the upper metal line region 61 is filled to form an upper metal line (not shown).

As discussed earlier, in accordance with the present invention, the lower metal line exposed through the via contact hole is covered by the photoresist pattern so that the edge of an interlayer insulating film at the top corner of the via contact hole is not etched during a formation process of upper metal line region. This prevents short between the metal lines caused by the reduction of distance therebetween, thereby improving the electrical

characteristics of semiconductor device.

As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiment is not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the metes and bounds of the claims, or equivalences of such metes and bounds are therefore intended to be embraced by the appended claims.